REMARKS

Claims 1-22 are pending, with claims 1, 9, 13, and 21 being in independent form. By the present amendment, claims 1, 3, 9, 13, and 21 have been amended.

In the Office Action, claims 1, 3-5, 13, and 15-17 stand rejected for anticipation by U.S. Patent No. 6,049,233 to Shurboff ("Shurboff"). Claims 6-8 and 18-20 stand rejected for obviousness over Shurboff and claims 2, 9-12, 14, 21, and 22 for obviousness over Shurboff in view of the publication "Phase-Locked Loop Phase Adjustment" by D.P. Turner ("Turner").

Applicant describes a phase-locked loop that includes a phase detector, a loop filter, a voltage controlled oscillator and a frequency divider arranged such that the phase detector generates a phase detector output signal as a function of a phase difference between the reference clock signal and the feedback signal. The phase-locked loop further includes one or more circuit elements that maintain an operating point of the phase detector such that, for a predetermined range of both positive and negative phase differences between the reference clock signal and the feedback signal, the output signal is generated as a substantially linear function of the phase difference between the reference clock signal and the feedback signal. As defined by claim 1, the substantial linearity of the output signal is due at least in part to a shifting of the operating point so that a zero output signal corresponds to a nonzero phase difference between the first and second signals.

The operating point circuit may assume any of a number of alternative embodiments. For example, the operating point circuit may leak a predefined portion of the output signal so as to prevent the leaked output signal from influencing the output frequency of the phase-locked loop. Alternatively, a delay circuit may be used to delay only one or both of first and second charge pump control signals from being supplied to the reset logic. If both the first and second charge pump control signals are delayed, a different delay time is used for each.

As described in the specification on page 12, lines 5-13, the asymmetric delay in the reset path corresponds to fractional-N divider jitter. In practice, this jitter is, for example, approximately 3 RF cycles, or 1.6 - 3.3ns for RF frequencies in the range 900-1800MHz (such as in a GSM system). According to claim 1, the phase detector output is linear with respect to the phase difference between the first and second

signals (as illustrated by Fig. 11, for example). As illustrated by Fig. 10, an up-down current balance in the phase detector prevents noise folding. In practice, however, a small imbalance will exist (see Fig. 6) and delta-sigma induced phase jitter (see Fig. 9) will cause noise folding even when the up-down current pulses are timed accurately. That is, when the reference leads the feedback signal by a certain amount, the error current is not identical in magnitude as in the case when the feedback leads the reference by the same amount.

To circumvent this even-order nonlinearity in the phase detector, the phase detector of claim 1 shifts the operating point of the phase detector so that a zero output signal corresponds to a nonzero phase difference between the first and second signals. This moves the operating region for the delta-sigma jitter, *during phase-locked conditions*, to one charge pump side (as illustrated by Fig. 11, for example).

To support a rejection under 35 U.S.C. § 102, each and every feature of the claimed invention must be shown in a single prior art document. Moreover, to establish a prima facie case of obviousness, the cited documents must teach or suggest all of the claim limitations. As discussed below, the pending claims positively recite limitations that are not disclosed nor suggested in the cited documents and are therefore not anticipated by, nor obvious in view of the cited documents.

Shurboff does not disclose nor suggest an operating point circuit that maintains an operating point of the phase detector such that for a predetermined range of both positive and negative phase differences between the first and second signals, the output signal is generated as a *substantially linear function* of the phase difference between the first signal and the second signal, as defined by claim 1.

Moreover, Shurboff does not disclose nor suggest that the substantial linearity of the output signal is due at least in part to a shifting of the operating point so that a *zero output signal corresponds to a nonzero phase difference* between the first and second signals, as defined by claim 1. In contrast, Shurboff states that "there is a need in the art for a phase detector which provides equal amounts of charge to the loop near the in-phase condition" (col. 1, lines 42-44). Shurboff also states, "with the loop in lock,...the phase detector circuit 500 generates substantially equal up current

and down current pulses" (col. 5, lines 55-58). That is, in Shurboff, when the net current is zero, i.e., the output signal is zero, the phase loop is locked, i.e., the phase difference is zero.

In contrast, in claim 1, a *zero output signal corresponds to a nonzero phase difference*. The delay asymmetry is chosen to shift the operating point away from the origin of the phase detector transfer function (phase difference vs. output signal), as illustrated by Fig. 11 and described on page 11, lines 3-14, in the application.

Nowhere in Shurboff is this feature disclosed or suggested. Instead, Shurboff discloses a transfer function that passes through the origin, i.e., the output signal is zero when the phase difference is zero. Accordingly, Shurboff could not possibly avoid nonlinearities in the transfer function, as in the claim 1. Not surprisingly, the importance (or even existence) of a linear output signal vs. phase difference relation is not disclosed anywhere in Shurboff.

Furthermore, as can be appreciated by one of skill in the art, the unduly large delay asymmetry of 20ns disclosed in Shurboff (col. 5, ll. 8-10, also col. 6, ll. 62-66) will not result in substantial linearity of the output signal but will instead impair loop performance with respect to locking range and capture range. For example, the 20ns delay asymmetry in Shurboff far exceeds (by an order of magnitude) the 1.6 - 3.3ns needed to maintain substantial linearity of the output signal for RF frequencies in the range 900-1800MHz (such as in a GSM system).

Independent claims 9, 13, and 21 include analogous distinguishing features.

Turner does not cure the aforementioned deficiencies.

Accordingly, since the cited documents, alone or in combination fail to disclose or suggest all of the claim limitations for at least the above reasons, both the anticipation and the obviousness rejections of the pending claims should be withdrawn.

For the foregoing reasons, Applicants consider the application to be in condition for allowance and respectfully request notice thereof at an early date. The Examiner is encouraged to telephone the undersigned at the below-listed number if, in the Examiner's opinion, such a call would aid in the examination of this application.

Respectfully submitted,

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